
	Hashemite University	
	Prince Al-Hussein bin Abdullah II Faculty for Information Technology	
	Department of Computer Science and its Applications	

## Course Syllabus

Year: 2018-2019

Semester: (2)

Course No.	Course Title	Designation	Prerequisite	Co-requisite	Credit Hours Lectures /Lab.
1510011123	Digital Logic Design	Required	110101152	-	3 / 0

Instructor Name	E-mail	Office No.	Office ext.	Office Hours
Dr. Sari Awwad	<a href="mailto:sari@hu.edu.jo">sari@hu.edu.jo</a>	124	-	All days (10-11)
Dr. Ahmad Qawasmeh	<a href="mailto:AhmadR@hu.edu.jo">AhmadR@hu.edu.jo</a>	236	-	Sun, Tue, Thu (10-11)

<b>Coordinator's Name:</b>	Dr. Sari Awwad
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<b>Course Description</b>	This course the following topics are introduced. Digital and numbering systems: conversion methods, binary and complement arithmetic; Boolean algebra; Circuit minimization techniques; Combinational circuits: Adders, Decoders, Encoders, Code Converters; Sequential Circuits: flip-flops, counters, registers, synchronous sequential circuits.
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<b>a) Textbook (s):</b>
1. Morris Mano and Michael D. Ciletti, Digital Design, 5th Edition, Prentice Hall, 2013., ISBN-10: 0-273-76452-7; ISBN-13: 978-0-273-76452-6
<b>b) Additional References:</b>
1. Digital Logic Design, Fourth Edition by <a href="#">Brian Holdsworth</a> and <a href="#">Clive Woods</a> , 2002.
2. Fundamentals of Logic Design by Charles H and Roth, Jr. West Publishing Company

<b>Course Learning and Outcomes CLOs</b>
1. Recognize the numbering systems and digital logic circuits. (2 ABET)
2. Analyze a logic circuit, and identify and define its inputs/outputs (1 ABET)
3. Analyze and design logic networks using both traditional techniques (such as K-maps and state tables) and modern CAD tools. (2 ABET)
4. Design, implement, and evaluate a digital circuit (2 ABET)
<b>Addressed Student Learning Outcomes (SLOs)</b>
1 and 2(ABET)

<b>Topic Details</b>	<b>Course ILO number</b>	<b>Reference</b>	<b>No. of Weeks</b>	<b>Contact hours*</b>
1. Digital and Numbering Systems:	1	Ch1	2	6
2. Boolean Algebra and Logic gates:	2	Ch2	3	9
3. Gate-Level Minimization	2	Ch3	2	6
4. Combinational Logic	3	Ch4	3	9
5. Synchronous Sequential Logic	4	Ch5	3	9
6. Registers and Counters	4	Ch6	2	6
Total			15	45

<b>Assessment method</b>	<b>Grade</b>	<b>Comments</b>
First Exam	30%	Covers Chapters 1, 2
Second Exam	30%	Covers Chapters 3, 4
Final Exam	40%	Covers all topics
Total	100%	